Soham Sanjay Dekhane

Weingarten, Germany
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Personal Website, LinkedIn

Skills

VHDL
Verilog
FPGA
Specman e
System Verilog
Ruby
Xilinx Vivado
Quartus
Modelsim
KiCad
Cadence Xcelium
C
LaTeX
MS Office

Languages

Deutsch
English
Marathi
Hindi

Hobbies

Formula 1, Traveling, Photography, Badminton, Reading about new and upcoming technologies

Education

M.Eng. Electrical Engineering and Embedded Systems, Hochschule Ravensburg-Weingarten, Weingarten, Deutschland
September 2021 — October 2023

B.Tech. Electronics and Telecommunication Engineering, Symbiosis International (Deemed) University, Pune, India
July 2017 — May 2021

Employment History

Master's Thesis, Hochschule Ravensburg-Weingarten, Weingarten
April 2023 — October 2023

- Implementing a Pseudo-Random-Number-Generator using a LFSR on a
- (MicroSemi) FPGA.
- Making the design scan testable (DFT - Design-for-Test). Integration of a JTAG-TAPC on the chip.
- Securing the device against threads from the debug interface (DFS - Design-for-Security).
- Planning and specifying the design with respect to DFT (already state of the art), DFD (also state of the art) and DFS (in research).
- Implementing this device and setting up the pure functional test and second, the scan-test on the EVA100

Werkstudent, Infineon Technologies AG, München
October 2022 — March 2023

- Implemented the testcase for verifying the register resets on the SRAM Support Hardware using Specman e.
- Implemented the test case on 1 register field and automated the generation of the testcase for 40+ other register fields using the register XML file and Ruby.
- Implemented the coverage scenario for the testcase and performed a clean regression run.

Intern – Hardware Design, BitMapper Integration Technologies Pvt. Ltd., Pune
January 2020 — June 2020 & July 2021 — August 2021

- Designed FPGA based ruggedized systems for Indian Defense and Space in areas like signal processing, image processing.
- Worked on areas like analysis, design, verification, project testing, quality assurance & defect fixes.
- Worked with 7-series Xilinx FPGAs and SoCs.
- Schematic design & verification.

Research Assistant, Hochschule Ravensburg-Weingarten, Weingarten
April 2022 — August 2023

- Working on the Advantest EVA-100 SoC testing kit.
- Preparing documentation for testing Analog as well as digital circuits on the testing kit.
- Helping students in doing their Bachelor's Thesis on the EVA-100 kit.

Projects

8-bit MCU VHDL implementation

- Making entity declarations for all the modules of the MCU provided by the professor.
- Linking different modules to realise the design for CPU and memory.
- Linking all the modules together to realise the top level module for the 8-bit MCU

Early Stage Brain Tumor Detection & Segmentation using Image Processing & Machine Learning

- Designed a SVM based model for detection of Brain tumor from MRI scans. Developed an Algorithm for segmentation of Brain Tumor.
- Curated data through the BraTS 2018 database.
- Coordinated with the project guide and worked on defect fixing. Achieved a testing accuracy of 87.88%.

I hereby declare that the details and information given above are complete and true to the best of my knowledge.

Weingarten, 28th November 2023

Place, Date, Signature